Sai Harsha Nimmagadda

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SUMMARY

Ph.D. researcher in Computer Engineering with a strong foundation in embedded firmware, wireless systems, design and optimization techniques. Combines integrated sensing and communications research with data analysis and system-level design to develop efficient hardware and software solutions. Seeking challenging internship opportunities from January 2027.

EDUCATION

Doctor of Philosophy (PhD) in Computer Engineering Expected Dec 2028
Arizona State University, Tempe, AZ GPA: 3.64
Coursework: VLSI design, Advanced computer architecture, CMOS digital systems & circuits, Semiconductor device physics.
Master of Science in Computer Engineering (Electrical Engineering) May 2023
Arizona State University, Tempe, AZ GPA: 3.57

SKILLS

Technology node and programming skills: 7nm, 12nm, 15nm, 16nm, 32nm, Python, Verilog, LabVIEW, Tcl, MATLAB.
Development skills: Electronic circuit design, hardware architecture, component selection, schematic interpretation, hardware debugging, embedded firmware, wireless edge monitoring, energy-aware transmission scheduling, power analysis, signoff analysis, QoR assessment, design automation, validation, circuit design, transistor-level simulation, RTL design, performance, LCN, communication quality-of-service analysis and area analysis.
EDA tools and OS: Cadence (Genus, Innovus, Virtuoso), Mentor Graphics (ModelSim, Calibre), Xilinx Vivado, Windows, Linux, GTKWave, Microsoft Office.

EXPERIENCE

Graduate Research Assistant | Arizona State University Jan 2026 – Present
Class-Aware Reinforcement Learning Analysis for Energy-Harvesting IoT Networks
- Designed a class-aware experimental study for 40 energy-harvesting IoT devices, grouping nodes into dynamically changing environmental classes across 30 learning epochs and monitoring devices through LCN.
- Developed AI-driven edge monitoring with energy awareness and a reliable system through reinforcement learning.
- Implemented constrained Q-learning on embedded firmware (nRF7002) to optimize node transmission scheduling, reducing network penalty and improving QoS by 30% under energy constraints.
- In collaboration with **NSF** funded project, **Factory-AI**, contribute machine learning and embedded-systems expertise to AI-driven edge intelligence for industrial wireless data collection.

IC Design Engineer | Western Semiconductor Feb 2024 – Aug 2024
- Designed standard cells, memory bitcells at transistor level, gate level in TSMC 16nm process using in-house EDA tools.
- Performed synthesis on 16KB SRAM using 6T for single port configuration ensuring data detection and optimized PPA.

IC Design Intern | Western Semiconductor Dec 2023 – Jan 2024
- Designed standard cells, high speed flops at transistor level, gate level in TSMC 12nm process using in-house EDA tools.
- Implemented standard-cell layout physical verification (DRC), fixed bugs to meet PDK runset and block-level requirements.

Graduate Research Assistant | Arizona State University May 2022 – May 2023
- Developed secure design using OpenCell library on 15nm to ensure hardware security, power, performance, and area.
- Optimized datapath timing by implementing pipelining, verified RTL simulation and post-synthesis gate-level netlist.
- Strengthened incremental floorplan at chip level, block level and implemented PnR to achieve max frequency 250 MHz.

Data Analyst | Cognizant Technology Solutions Jun 2020 – Jul 2021
- Implemented GSD management using Python to retrieve data and processed data to analyze behavior of design.
- Collaborated with cross-functional teams to identify the root cause for customer queries and achieved 95% efficiency.

ACADEMIC PROJECTS

TinyML Steel-Defect Classification on an Embedded IoT Node Fall 2026
- Trained and deployed TinyResNet model for six-class steel surface defect classification on nRF5340 node. Reduced the model to 14,270 parameters, approximately 13.8 KB of quantized weights, and 25.6 KB of static activation memory.
- Quantized and deployed model on nRF5340, achieving 97.4% test accuracy and 99.6% prediction agreement with the original floating-point model on 270 held-out images.

FastComm: Energy-Aware Adaptive Wireless IoT Testbed Spring 2026
- Developed embedded firmware for an adaptive wireless IoT testbed using Zephyr RTOS, Nordic nRF5340/nRF7002 hardware, Wi-Fi, TCP/UDP and MQTT.
- Implemented on-device Q-learning communication through Distributed control systems (DCS) policy that selects packet count and transmission phase using packet reliability, Age of Information, energy availability, and channel load.
- Achieved extended coverage of 200 m and reduced production cost to require more access points, with a latency of 14 ms.